REMARKS

Applicants respectfully requests consideration and allowance of claims 1, 3-9, 11-16, 18-26, and 28-35 that are pending in the above-identified patent application. Applicants have amended claims 1, 3-9, 13-16, 20-22, 25, 26, 28-30, and 35. Claims 2, 10, 17 and 27 are canceled. Support for the amendments can be found in the specification as filed at Fig. 3 and related description at paragraphs [0035] and [0036]. No new matter has been added by way of these amendments.

I. Rejection of Claims 30, 35 Under 35 U.S.C. §101:

At numbered part 3 of the Office Action, the Examiner has rejected claims 30, 35 under 35 U.S.C. §101 as allegedly being directed towards non-statutory subject matter. In particular, it is contended that since the claims recite "a processor control program" they are non-statutory. These rejections should be withdrawn for at least the following reasons. Claims 28, 30 and 35 have been amended so that they are now directed towards a processor readable memory having stored thereon instructions for carrying out the claimed steps. In view of these amendments, it is submitted that the claims are now directed towards statutory subject matter and hence this rejection should be withdrawn. Support for the amendments can be found in the specification as filed at Fig. 1, and paragraphs [0030], [0031].

II. Rejection of Claims 1-2, 4, 9-10, 12, 16-17, 19, 21-22 and 24 Under 35 U.S.C. §102(b):

At numbered parts 4-10 of the Office Action, the Examiner has rejected claims 1-2, 4, 9-10, 12, 16-17, 19, 21-22 and 24 under 35 U.S.C. §102(b) as being anticipated by Luick (U.S. 20030229662). Applicant respectfully traverses this rejection and submits that this rejection should be withdrawn for at least the following reasons. Luick does not disclose an identical invention as recited in the instant claims.

The claimed subject matter generally relates to a processor for controlling performance in accordance with a chip temperature. To this end, independent claim 1 recites: consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of

operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature. Independent claim 9 recites in addition to the aforementioned aspect: a control unit which consults the table and switches between the operation points in accordance with the measured temperature. Independent claims 16 and 21 recite features similar to independent claim 9. Luick does not disclose such claimed aspects.

Luick relates to eliminating hot spots on processor chips in a symmetric multiprocessor (SMP) computer system. When a hot spot occurs, on a processor tasks as swapped to another processor prior to the localized temperature becoming too hot. Moving of tasks to processors that have data affinity with the processor reporting a hot spot is one of the considerations. Further considerations include prioritizing unused processors and those processors that have not recently reported a hot spot. (*See* Luick Abstract). Accordingly, Luick discloses hot processor registers (HPR), which store information about which processors in the SMP have reported hot spots, and when the hot spots occurred. A timer is used to generate a "time stamp" when a hot spot has been reported. The operating system utilizes the information regarding which processors have reported hot spots and when the hot spots occurred to move a task that has caused a hot spot to a processor that has not reported a hot spot for a long period of time (*See* Luick paragraph [0062]). Thus, Luick discloses a hot processor register (HPR) that keeps a record of when and which processors have developed hot spots. This is not identical to a table that that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature as recited in independent claim 1 and other independent claims 9, 16 and 21.

In accordance with an embodiment of the claimed subject matter, if the estimated temperature of a processor system is higher than or equal to a predetermined threshold temperature, the temperature control unit acquires the number of sub processors available in parallel after that period Δt from the task management unit. The temperature control unit then consults the performance table and identifies the candidate of the operation point from the performance table. It also acquires the number of sub processors to operate and the operating

frequency of the processor at that operation point, and passes the same to the heat generation amount estimation unit. The candidate operation point is changed based on the result from the heat generation estimation unit.
(*See* Applicants' specification as filed paragraphs [0057] – [0060]). Therefore, it is submitted that Luick fails to anticipate the aforementioned independent claims and claims 2, 4, 10, 12, 17, 19, 22 and 24 depending therefrom.

In addition independent claims 9, 16 and 21 also recite a control unit which consults the table and switches between the operation points in accordance with the measured temperature. As Luick fails to disclose a table comprising entries which are combinations of the number of processing blocks formed inside a processor and in operation; and one of a plurality of operating frequencies available for use, it follows that it also fails to disclose a control unit that switches between such operation points as further recited in claims 9, 16 and 21.

In view of at least the foregoing, it can be concluded that the cited art does not disclose an identical invention as recited in the subject independent claims. Hence, this rejection should be withdrawn with respect to these claims as well as claims that depend from them.

III. Rejection of Claims 13-15, 20, 25-26, 28-29, and 35 Under 35 U.S.C. §102(b):

At numbered parts 11-19 of the Office Action, the Examiner has rejected claims 13-15, 20, 25-26, 28-29, and 35 under 35 U.S.C. §102(b) as allegedly being anticipated by Hirai et al. (U.S.20050278520). This rejection should be withdrawn for at least the following reasons. Hirai et al. fails to disclose an identical invention as recited in the subject claims.

The claimed subject matter generally relates to controlling performance of a processor in accordance with a chip temperature. To this end, independent claim 13 recites: a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching; and a control unit which consults the table and switches between the operation points as appropriate. Independent claims 20, 25 recite similar features. Independent claim 26 recites: consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor in operation; and b)

one of a plurality of operating frequencies available for use by switching, and switching between the operation points in accordance with a temperature. Hirai et al. does not disclose such aspects.

Hirai et al. provides for a task scheduling apparatus of a distributed processing system having a plurality of processing units for processing a plurality of distributed tasks. Initially, the task scheduling apparatus allocates a task to a processing unit having the lowest temperature. As a second scheduling task, the task scheduling apparatus selects a task based on both temperature of each processing unit and characteristic values of tasks related to degree of temperature rise or consumption power increase caused by execution, and allocates the selected task to the object processing unit. However, it fails to disclose a table which lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks in operation; and b) one of a plurality of operating frequencies available for use by switching. Consequently, Hirai et al. also fails to disclose a control unit which consults the table and switches between the operation points as appropriate.

In addition, dependent claim 14 further recites that the table lists the operation points in order of performance. This further facilitates selecting an appropriate combination of sub-processors and operating frequencies for switching. Hirai et al. only discloses switching tasks based on current temperature of processor or anticipated temperature rise due to the task, but does not teach or suggest a table as recited in dependent claim 14.

In view of at least the foregoing, it can be concluded that Hirai et al. fails to anticipate independent claims 13, 20, 25 and 26. Hence, this rejection should be withdrawn with respect to these claims as well as claims 14, 15, 28, 29, and 35 that depend from them.

IV. Rejection of Claims 3, 11, 18, 23 and 31-34 Under 35 U.S.C. §103(a):

At numbered parts 20-23 of the Office Action, the Examiner has rejected claims 3, 11, 18, 23 and 31-34 Under 35 U.S.C. §103(a) as being obvious over Luick in view of Guo et al. (U.S. 20050071843). Applicants traverse the rejection and submit that this rejection should be withdrawn for at least the following reasons. Luick in view of Guo et al., alone or in combination, fail to teach or suggest all aspects recited in independent claims.

Claims 3, 11, 18, 23 and 31-34 depend from independent claims 1, 9, 16, 21 and 26. The deficiencies of the Luick as concerns these independent claims were discussed above. As the teachings of the Guo et al. that the Examiner alleges is combinable with Luick do not cure such deficiencies, Applicants respectfully request that the obviousness rejection of the subject claims be withdrawn. More particularly, Guo et al. relates to scheduling jobs in a multiprocessor machine. The jobs are scheduled by comparing resource requirements of jobs against resources available to particular CPUs. However, alone or in combination with Luick it fails to teach or suggest consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points in accordance with a temperature or a control unit which consults the table and switches between the operation points in accordance with the measured temperature. In view of at least the foregoing, it is requested that this rejection should be withdrawn.

V. Rejection of Claims 5-8 and 30 Under 35 U.S.C. §103(a):

At numbered parts 24-29 of the Office Action, the Examiner has rejected claims 5-8 and 30 under 35 U.S.C. §103(a) as being obvious over a combination of Luick and Chauvel et al. (U.S. 7062304). This rejection should be withdrawn for at least the following reasons. Luick and Chauvel et al. alone or in combination do not teach or suggest all aspects recited in independent claims 5 and 30.

As discussed herein, the claimed subject matter relates to a processor for controlling performance in accordance with a chip temperature, and a method of controlling the processor. To this end, independent claim 5 recites: consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, so as to switch between the operation points. Similarly independent claim 30 recites: consulting a table that lists a plurality of operation points defined by combinations each comprising: a) the number of processing blocks formed inside a processor in operation; and b) one of a plurality

of operating frequencies available for use by switching, and switching between the operation points. The cited art does not teach or suggest such claim aspects.

The deficiencies of the Luick as concerns these independent claims were discussed above. As the teachings of Chauvel et al. that the Examiner alleges is combinable with Luick do not cure such deficiencies, Applicants respectfully request that the obviousness rejection of the subject claims be withdrawn. More particularly, Chauvel et al. relates to a multiprocessor system that includes a plurality of processing modules, such as MPUs, DSPs, and coprocessors/DMA channels. Power management software in conjunction with profiles for the various processing modules and the tasks to execute are used to build scenarios which meet predetermined power objectives, such as providing maximum operation within package thermal constraints or using minimum energy. Actual activities associated with the tasks are monitored during operation to ensure compatibility with the objectives. The allocation of tasks may be changed dynamically to accommodate changes in environmental conditions and changes in the task list. (*See* Chauvel et al. Abstract). At the cited portions Chauvel et al. discloses that the model can consist of a family of curves that represent MPU (microprocessor units) or DSP effective frequency variations with different parameters, such as data cacheable/non-cacheable, read/write access shares, number of cycles per instruction, and so on. (*See* Chauvel et al. col. 6 lines 35-40). Thus, Luick discloses a hot processor register that keeps a record of hot spots developing in processors and Chauvel et al. discloses curves that show variations of effective frequency of processors with different factors none of which include combinations of the number of processing blocks formed inside a processor with operating frequencies. Therefore, even if Luick and Chauvel et al. are combined, the combination would not result in the claimed subject matter. As the combination of Luick and Chauvel et al. fails to disclose any structure meeting the combinations each comprising: a) the number of processing blocks formed inside a processor and in operation; and b) one of a plurality of operating frequencies available for use by switching, the Examiner's allegation requires imbuing the cited art with subject matter that does not exist.

In addition, dependent claim 6 recites an additional aspect of the table listing the plurality of operation points in the order of processing performance. This facilitates selection of operation

points for switching. The cited art also fails to teach or suggest this aspect. In view of at least the foregoing it is respectfully submitted that the cited art fails to disclose all aspects recited in the independent claims 5, 30. Hence, this rejection should be withdrawn with respect to these claims as well as claims 6-8 depending there from.

VI. Rejection of Claim 27 Under 35 U.S.C. §103(a):

At numbered parts 30-31 of the Office Action, the Examiner has rejected claim 27 under 35 U.S.C. §103(a), as allegedly being obvious over Hirai as applied to claims 25-26 and Luick. This rejection should be withdrawn as claim 27 is canceled.

Conclusion:

In view of the foregoing, Applicant respectfully submits that the instant application is in condition for allowance. Early and favorable action is earnestly solicited.

In the event there are any fees due and owing in connection with this matter, please charge same to our Deposit Account No. 11-0223.

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Respectfully submitted,

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